Analog Electronics Circuits

FET small signal Analysis

- FET introduction and working principles
- FET small signal analysis
- FET self bias technique.
- Examples
- JFET self bias configuration
- Numerical
- JFET Voltage divider configuration
- JFET common drain configuration
- Source follower.
- Numerical
- JFET common gate
- Depletion mode
- Enhancement mode
- E MOSFET drain feedback configuration.
- E MOSFET voltage divider Configuration.
- numerical
FET Introduction

- *The Field-Effect Transistor* (FET) is a type of transistor that works by modulating a microscopic electric field inside a semiconductor material.

- There are two general type of FET's, the MOSFET and JFET.

Symbol and representation

![FET Symbol and Representation](image-url)

**JFET Construction**

There are two types of JFET’s: n-channel and p-channel. The n-channel is more widely used.

![JFET Construction Diagram](image-url)
Basic operation of JFET

- The JFET operation is compared with the water spigot.

The source of water pressure

- accumulated electrons at the negative pole of the applied voltage from Drain to Source

The drain of water

- electron deficiency (or holes) at the positive pole of the applied voltage from Drain to Source.

The control of flow of water

- Gate voltage that controls the width of the n-channel, which in turn controls the flow of electrons in the n-channel from source to drain.

JFET Operating Characteristics

There are three basic operating conditions for a JFET:

A. $V_{GS} = 0$, $V_{DS}$ increasing to some positive value

B. $V_{GS} < 0$, $V_{DS}$ at some positive value

C. Voltage-Controlled Resistor
A. VGS = 0, VDS increasing to some positive value

Three things happen when VGS = 0 and VDS is increased from 0 to a more positive voltage:

- The depletion region between p-gate and n-channel increases as electrons from n-channel combine with holes from p-gate.
- Increasing the depletion region, decreases the size of the n-channel which increases the resistance of the n-channel.
- But even though the n-channel resistance is increasing, the current (ID) from Source to Drain

  Through the n-channel is increasing. This is because VDS is increasing.
Pinch off

Saturation
At the pinch-off point:

- any further increase in VGS does not produce any increase in ID. VGS at pinch-off is denoted as $V_p$.
- ID is at saturation or maximum. It is referred to as $IDSS$.
- The ohmic value of the channel is at maximum.

**B. $V_{GS} < 0$, $V_{DS}$ at some positive value**

As $V_{GS}$ becomes more negative the depletion region increases.
Now $I_d < I_{dss}$

As $V_{GS}$ becomes more negative:

- the JFET will pinch-off at a lower voltage ($V_p$).
- $I_D$ decreases ($I_D < I_{dss}$) even though $V_{DS}$ is increased.
- Eventually $I_D$ will reach 0A. $V_{GS}$ at this point is called $V_p$ or $V_{GS}(off)$.

Also note that at high levels of $V_{DS}$ the JFET reaches a breakdown situation. $I_D$ will increases uncontrollably if $V_{DS} > V_{DS_{max}}$

C. Voltage-Controlled Resistor

- The region to the left of the pinch-off point is called the *ohmic region*.
- The JFET can be used as a variable resistor, where $V_{GS}$ controls the drain-source resistance ($r_d$).
- As $V_{GS}$ becomes more negative, the resistance ($r_d$) increases.
Transfer Characteristics

- The transfer characteristic of input-to-output is not as straightforward in a JFET as it was in a BJT.

- In a BJT, β indicated the relationship between IB (input) and IC (output).

- In a JFET, the relationship of VGS (input) and ID (output) is a little more complicated:

  Current relation

\[
I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2
\]

Comparison between BJT & FET
<table>
<thead>
<tr>
<th>BJT</th>
<th>FET</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. BJT controls large output ($I_C$) by means of a relatively small base current. It is a current controlled device.</td>
<td>1. FET controls drain current by means of small gate voltage. It is a voltage controlled device</td>
</tr>
<tr>
<td>2. Has amplification factor $\beta$</td>
<td>2. Has trans-conductance $g_m$.</td>
</tr>
<tr>
<td>3. Has high voltage gain</td>
<td>3. Does not have as high as BJT</td>
</tr>
<tr>
<td>4. Less input impedance</td>
<td>4. Very high input impedance</td>
</tr>
</tbody>
</table>

FET Small-Signal Analysis

- FET Small-Signal Model
- Trans-conductance

The relationship of $V_{GS}$ (input) to $I_D$ (output) is called trans-conductance.

- The trans-conductance is denoted $g_m$.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Definition of $g_m$ using transfer characteristics
Example:

Determine the magnitude of $g_m$ for a JFET with $I_{DSS} = 8mA$ and $V_P = -4V$ at the following dc bias points.

a. At $V_{GS} = -0.5V$

b. At $V_{GS} = -1.5V$

c. At $V_{GS} = -2.5V$
Mathematical Definition of \( g_m \)

\[
g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{\partial I_D}{\partial V_{GS}}
\]

\[
I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2
\]

\[
g_m = \frac{2I_{DSS}}{|V_P|} \left[1 - \frac{V_{GS}}{V_P}\right]
\]

\[g_m \text{ for } V_{GS} = 0V: \quad g_{m0} = \frac{2I_{DSS}}{|V_P|}\]

\[
1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}
\]

\[
g_m = g_{m0} \sqrt{\frac{I_D}{I_{DSS}}}
\]

---

**FET Impedance**

- Input Impedance \( Z_i \): \( \infty \) ohms
- Output Impedance \( Z_o \): \( r_d = 1/yos \)

\[
I_d = \frac{\Delta V_{DS}}{\Delta I_D} \bigg|_{V_{GS} = \text{constant}}
\]

Yos = admittance equivalent circuit parameter listed on FET specification sheets.
Two port model

FET AC Equivalent Circuit

Phase Relationship

- The phase relationship between input and output depends on the amplifier configuration circuit.
- Common – Source ~ 180 degrees
- Common - Gate ~ 0 degrees
- Common – Drain ~ 0 degrees
JFET Common-Source (CS) Fixed-Bias Configuration

• The input is on the gate and the output is on the drain.

• Fixed bias configuration includes the coupling capacitors c1 and c2 that isolate the dc biasing arrangements from the applied signal and load.

• They act as short circuit equivalents for the ac analysis.

AC Equivalent Circuit

\[
Z_{i} = R_G \\
Z_{o} = r_d \cdot R_D
\]

\[
Z_{o} \approx R_D \mid I_d \geq 10R_D
\]
Voltage gain

\[ A_v = \frac{V_o}{V_i} = -g_m R_D \quad | \quad r_d \geq 10R_D \]

\[ A_v = \frac{V_o}{V_i} = -g_m (r_d \parallel R_D) \]

Phase difference

Negative sign in the gain expression indicates that the output voltage is 180° phase shifted to that of input.

Example

For fixed bias circuit, the following bias data are given. \( V_{GS} = -2V \), \( I_{DO} = 5.625mA \) and \( V_p = -8V \). The input voltage \( v_i \). The value of \( y_{OS} = 40 \mu S \).

1. Determine \( G_m \)
2. Find \( r_d \)
3. Determine \( Z_i \)
4. Calculate \( Z_O, A_V \) with and without effects of \( r_d \).
JFET Self bias configuration

- Main disadvantage of fixed bias configuration requires two dc voltage sources.
- Self bias circuit requires only one DC supply to establish the desired operating point.

Self bias configuration

If Cs is removed, it affects the gain of the circuit
AC Equivalent Circuit

- The capacitor across the source resistance assumes its short circuit equivalent for dc allowing $R_S$ to define the operating point.
- Under ac conditions the capacitors assumes short circuit state and short circuits the $R_S$.
- If $R_S$ is left un-shorted, then ac gain will be reduced.
Redrawn equivalent circuit:

Here $R_s$ is bypassed by $X_{CS}$

Circuit parameters:

- Since the resulting circuit is same as that of fixed bias configuration, all the parameter expression remains same as evaluated for fixed bias configuration.

- Input impedance $Z_i = R_G$

- Output Impedance: $Z_o = r_d$ parallel $R_D$

\[ Z_o \approx R_D \mid I_d \geq 10R_D \]

Leaving $R_s$ un-bypassed helps to reduce gain variations from device to device by providing degenerative current feedback. However, this method for minimizing gain variations is only effective when a substantial amount of gain is sacrificed.
Self bias configuration with un bypassed $R_s$

Here $R_s$ is part of the equivalent circuit.

There is no way to reduce the network with lowest complexity.

Carefully all the parameters have to be calculated by considering all polarities properly.

**Input Impedance**

- Due to open-circuit condition between gate and output network, the input impedance remains as follows:

$$Z_i = R_G$$

**Output impedance**
Output impedance is defined by

\[ Z_O = \frac{V_O}{I_O} \text{ at } v_i=0 \]

Setting \( v_i=0 \) results in the following circuit.

\[
\begin{align*}
Z_o &= \frac{RD}{1 + gmRs + \frac{RD + Rs}{rd}} \\
rd &> 10(RD + Rs) \\
Z_o &= \frac{RD}{1 + gmRs}
\end{align*}
\]

**Voltage gain:**

\[
Av = \frac{V_O}{V_i} = \frac{gmRD}{1 + gmRs + \frac{RD + Rs}{rd}}
\]

\[
rd \geq 10(RD + Rs), \quad Av = -\frac{gmRD}{1 + gmRs}
\]
Example: A self bias circuit has operating point defined by \( V_{GS_0} = -2.6V \), \( I_D = 2.6mA \) with \( I_{DSS} = 8mA \) and \( V_p = -6V \). \( Y_{os} = 20\mu S \)

Determine

a. \( G_m \)

b. \( R_d \)

c. \( Z_i \)

d. \( Z_o \) with and without \( r_d \) effect.

e. \( A_v \) with and without \( r_d \) effect
JFET voltage divider configuration

AC equivalent circuit

Input Impedance: $Z_i = R_1 \parallel R_2$

Output Impedance: $Z_o = r_d \parallel R_D$

$Z_o \approx R_D \bigg|_{r_d \geq 10R_D}$
Voltage gain:

\[ A_v = -g_m \left( r_d || R_D \right) \]

\[ A_v = -g_m R_D \bigg|_{r_d \geq 10R_D} \]

Note

- Equations for ZO and Av are same as in fixed bias.
- Only Zi is now dependent on parallel combination of R1 and R2.

**JFET source follower**
In a CD amplifier configuration the input is on the gate, but the output is from the source.

AC equivalent circuit

Input and output impedance:

- **Input impedance**: \( Z_i = R_G \)

- **Output impedance**: 
  
  setting \( V_i = 0 \text{V} \) will result in the gate terminal being connected directly to ground as shown in figure below.
Equivalent circuit

- Applying KCL at output node

\[ I_o + g_m V_{gs} = I_{rd} + I_{rs} \]

\[ = \frac{V_o}{r_d} + \frac{V_o}{R_s} \]

result: \[ I_o = V_o \left[ \frac{1}{r_d} + \frac{1}{R_s} \right] - g_m V_{gs} \]

\[ = V_o \left[ \frac{1}{r_d} + \frac{1}{R_s} \right] - g_m V_{gs} \]

\[ = V_o \left[ \frac{1}{r_d} + \frac{1}{R_s} \right] - g_m [-V_o] \]

\[ = V_o \left[ \frac{1}{r_d} + \frac{1}{R_s} + g_m \right] \]
\[ Z_o = \frac{V_o}{I_o} = \frac{V_o}{\left[ \frac{1}{r_d} + \frac{1}{R_s} + g_m \right]} \frac{1}{V_0} \]

\[ = \frac{1}{\left[ \frac{1}{r_d} + \frac{1}{R_s} + g_m \right]} \]

\[ Z_o \equiv R_s \parallel \frac{1}{g_m} \bigg|_{r_d \geq 10R_s} \]

rd, Rs and gm are all in parallel.

Voltage gain

\[ A_v = \frac{V_o}{V_i} = \frac{g_m (r_d \parallel R_s)}{1 + g_m (r_d \parallel R_s)} \]

\[ A_v = \frac{g_m R_s}{1 + g_m R_s} \bigg|_{r_d \geq 10R_s} \]

Since denominator is larger by a factor of one, the gain can never be equal to or greater than one. (as in the case of emitter follower of BJT)
Example:

A dc analysis of the source follower has resulted in $V_{GS}=-2.86\,V$ and $I_o=4.56\,mA$.

Determine

a. $g_m$

b. $Z_i$

c. $r_d$

d. Calculate $Z_o$ with and without effect of $r_d$.

e. Calculate $A_V$ with and without effect of $r_d$.

Compare the results.

Given $I_{DSS}=16\,mA$, $V_p=-4\,V$, $y_{os}=25\,\mu S$.

The coupling capacitors used are $0.05\,\mu F$.

JFET common gate configuration

The input is on source and the output is on the drain.
Same as the common base in BJT
AC equivalent circuit

Impedances:

Input Impedance: \( Z_i = R_s \parallel \frac{r_d + R_D}{1 + g_m r_d} \)

\( Z_i \approx R_s \parallel \frac{1}{g_m} \quad | \quad r_d \geq 10R_D \)

Output Impedance: \( Z_o = R_D \parallel r_d \)

\( Z_o \approx R_D \quad | \quad r_d \geq 10R_D \)
Voltage gain

\[ A_v = \frac{V_o}{V_i} = \frac{g_m R_D + \frac{R_D}{r_d}}{1 + \frac{R_D}{r_d}} \]

\[ A_v = g_m R_D \quad | r_d \geq 10 R_D \]
Example: For the network shown if $V_{GSo} = -2.2\, \text{V}$, $I_{Dq} = 2.03\, \text{mA}$,
Determine $g_m, r_d, Z_i$ with and without the effect of $r_d$, $A_v$ with and without the effect of $r_d$.
Also find $V_o$ with and without $r_d$. Compare the results.

$C_1$ and $c_2$ are given by $10\, \mu\text{f}$. 
MOSFETs:

MOSFETs are of two types;

- Depletion type
- Enhancement type

1. Depletion type MOSFETs

   - Shockley’s equation is also applicable to depletion type MOSFETs.
   - This results in same equation for gm.
   - The ac equivalent model for this MOS device is same as JFET.
   - Only difference is $V_{GS0}$ is positive for n-channel device and negative for p-channel device.
   - As a result of this, $gm$ can be greater than $gmo$. 
- Range of $r_d$ is very similar to that of JFETs.

**D-MOSFET ac equivalent model**

Example: A network shown below has the dc analysis results as $I_{DSS}=6\text{mA}$, $V_P=3\text{V}$, $V_{GSo}=1.5\text{V}$ and $I_{DQ}=7.6\text{mA}$. $y_{os}=10\mu\text{S}$

a. Determine $g_m$ and compare with $g_{mo}$

b. Find $r_d$

c. Sketch ac equivalent circuit

d. Find $Z_i$, $Z_o$ and $A_v$. 

[Diagram of D-MOSFET ac equivalent model]
Solution:

- \( \text{gmo} = 4 \text{mS} \)
- \( \text{gm} = 6 \text{mS} \)
- \( \text{gm} \) is 50% more than \( \text{gmo} \)
- \( \text{rd} = 100 \text{K} \)
- \( Z_i = 10 \text{M} \) parallel with 110M = 9.17M
- \( Z_o = 100 \text{K} \) parallel with 1.8K = 1.8K
- \( A_v = -\text{gmrd} = 10.8 \)

Ac equivalent circuits
Enhancement type MOSFET

- There are two types of E-MOSFETs:
  - nMOS or n-channel MOSFETs
  - pMOS or p-channel MOSFETs

E-MOSFET ac small signal model
• ID = k(VGS - VGS(Th))^2

• gm is defined by

• Taking the derivative and solving for gm,

\[ gm = 2k(VGS - VGS(th)) \]

EMOSFET drain feedback configuration
Ac equivalent model
Input and output impedances

Input Impedance: 
\[ Z_i = \frac{R_F + r_d \parallel R_D}{1 + g_m(r_d \parallel R_D)} \]

Output Impedance: 
\[ Z_o = R_F \parallel r_d \parallel R_D \]

\[ Z_i \approx \frac{R_F}{1 + g_m R_D} \]
\[ Z_o \approx R_D \]
\[ R_F \gg r_d \parallel R_D, \quad r_d \gg 10R_D \]

Voltage gain

\[ A_v = -g_m (R_F \parallel r_d \parallel R_D) \]

\[ A_v = -g_m R_D \]
\[ R_F \gg r_d \parallel R_D, \quad r_d \gg 10R_D \]
Numerical

For the above said configuration, the following results were got. K=0.24\times10^{-3}A/V^2, V_{gsQ}=6.4V, I_{DQ}=2.75mA. Determine \( g_m, r_d, Z_i \) with and without the effect of \( r_d \), \( Z_o \) with and without the effect of \( r_d \). \( A_V \) with and without effect of \( r_d \). And compare the results. \( I_d(sat)=6mA, V_{GS(th)}=3V, V_{GS(on)}=6V, y_{os}=20\mu S. \)

- \( R_D=2K \) ohms
- \( R_F=10M \) ohms
- \( C_1,c_2=1uF \)

Solution.

- \( g_m=2k(V_{GS}-V_{GS(th)}) =1.63mS. \)
- \( r_d=1/y_{os}=50K \)
- \( Z_i \) with \( r_d: \)

\[
Z_i = \frac{R_f + (r_d // R_D)}{1 + g_m(r_d // R_D)}
\]
= 2.42M

- Zi without effect of rd: 
  \[ Z_i = \frac{R_F}{1 + g_m R_D} \]
  = 2.53M

- Zo with rd: (R_F parallel \( r_d \) parallel R_D)
  = 1.92K

- Zo without rd: Zo=RD = 2K

- Gain A_V with \( r_d \):
  \[ A_V = -g_m \left( R_F \parallel r_d \parallel R_D \right) \]
  = -3.21

- Without effect of rd:
  \[ A_V \approx -g_m R_D \]
  = -3.26
E MOSFET voltage divider configuration

Important Parameters

Input Impedance: \[ Z_i = R_1 \parallel R_2 \]

Output Impedance: \[ Z_o = r_d \parallel R_D \]

\[ Z_o \equiv R_D \mid r_d \geq 10R_D \]

\[ A_v = -g_m (r_d \parallel R_D) \]

\[ A_v = -g_m R_D \mid r_d \geq 10R_D \]
Ac equivalent circuit